

REMARKS

By this Amendment, Applicants amend claims 1-3. Applicants also add new claims 13-15, and hence claims 1-15 are all the claims pending in the application.

Claim Rejections - 35 U.S.C. § 103

Claims 1-12 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Dahl et al. (U.S. Patent 5,710,938) in view of Toll (U.S. Patent 6,308,279). Applicants respectfully traverse the rejection.

Claims 1-3

The present invention is directed to an array-type processor in which a multiplicity of processor elements that each individually execute data processing, and for which the connection relations between the processor elements is switch-controlled are arranged in rows and columns, and in which the operations of the multiplicity of processor elements are controlled by a plurality of state control units.

The Examiner's position is that Dahl allegedly teaches substantially all the features of claims 1, 2, and 3. In particular, the Examiner asserts that figure 1 of Dahl allegedly teaches "an array-type processor comprising: a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, said multiplicity of processor elements arranged in rows and columns."

Dahl describes that figure 1 illustrates a data processing system having a plurality of message routing circuits coupled to form an array and a corresponding plurality of data processing nodes. *See* Dahl, col. 3, lines 32-39. However, Dahl also describes that "in actuality,

each data processing node includes a general purpose microprocessor...a memory...[and] a selectable number of peripheral input/output devices such as a disk, a tape, a keyboard, a CRT display, etc.” See Dahl, col. 3, lines 46-51. Indeed, Dahl discloses that “the microprocessor which is included in each of the nodes can be an Intel Pentium.” See Dahl, col. 10, lines 62-65.

Therefore, a person having ordinary skill in the art would understand that the “data processing nodes” of Dahl are, in fact, separate operational units each having their own microprocessor. As a result, Dahl neither teaches nor suggests “a multiplicity of processor elements...arranged in rows and columns **on the array-type processor**,” since the data processing system of Dahl is merely an arrangement of separate “data processing nodes,” with no teaching or suggestion of an array-type processor having a multiplicity of processor elements on the processor.

Accordingly, for at least these reasons, Dahl fails to teach or suggest all the features of claims 1-3. Toll is merely cited for teaching the halting of processors and also fails to teach or suggest the features discussed above. Accordingly, the combination of Dahl and Toll fails to teach or suggest all the features of claims 1-3, and hence claims 1-3 would not have been rendered unpatentable by the combination of Dahl and Toll.

Claims 4-12

Claims 4-12 depend on claims 1-3 and incorporate all the features of claims 1-3, and hence claims 4-12 should be deemed patentable at least by virtue of their dependency on claims 1-3.

New Claims

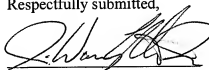
As discussed above, Applicants add new claims 13-15. Applicants respectfully submit that claims 13-15 should be deemed patentable at least by virtue of their dependency. Applicants also respectfully submit that the references cited by the Examiner fail to teach or suggest all the features of claims 13-15.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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